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Interface-Modified Ramp-Type Josephson Junctions in Trilayer Structures

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SUMMARY We have fabricated ramp-type Josephson junctions in trilayer structures. A bilayer of $YBa_2Cu_3O_{7-x}$ (YBCO)/CeO_2 was deposited on a $SrTiO_3$ (100) substrate. Then, circle patterns with a diameter of 2 μm were etched on the bilayer surface using standard photolithography process. During the Ar ion milling with an incident angle of 45 degrees to the bilayer surface, the sample was rotated. This process led to upside-down conical formations. After the ramp-edge surface was modified, another YBCO film was deposited for the top electrode. The junctions showed the *I-V* characteristics between resistively shunted junction and flux-flow types.

key words: *interface-modified, ramp-type, trilayer structures, Josephson junction*

1. Introduction

Josephson junctions are used as ultrahigh-speed switching devices in digital circuits based on single flux quantum logic. To manufacture large-scale digital circuits based on high-temperature superconductors, small spreads of Josephson junction parameters and reduced inductance values are very important.

High-quality Josephson junctions require very thin and uniform barrier layers. Barrier formation based on deposited materials has been studied in high-temperature superconducting junctions. However, it is difficult to deposit a uniform 2 to 3-nm-thick barrier layer. Interface modification technology, with which the barrier layers are formed by modifying the ramp edge surface, has greatly improved the spreads of the junction parameters [1], [2].

Ramp-type Josephson junctions have an advantage in that the current in the *ab*-plane can be utilized through making junctions along the *ab*-plane. However, their inductance values are still too large to be applied in the large-scale circuits, which is mainly due to parasitic inductances. Vertically stacked structures such as trilayer junctions contribute to both compact integration and reduced inductance values [3].

Hence, we propose a fabrication process for ramp-type Josephson junctions in trilayer structures which combines the advantages described above.

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2. Fabrication

$YBa_2Cu_3O_{7-x}$ (YBCO) and CeO_2 (CeO) thin films were prepared by the pulsed laser deposition (PLD) method. These films were deposited on the $SrTiO_3$ (STO) (100) substrate in order to grow YBCO films with *c*-axis orientation to the substrate surface. YBCO films were deposited at 720°C with 200 mTorr oxygen pressure. Critical temperatures of the films were 86 to 88 K. Subsequently, CeO films were deposited on the YBCO films at 650°C with 50 mTorr oxygen pressure. Post-annealing at 450°C in 1 atmosphere oxygen was carried out after the deposition of both films *in situ*.

A bilayer consisting of a 300-nm-thick YBCO film for the bottom electrode and a 230-nm-thick CeO insulation layer was prepared by the deposition processes mentioned above. The sixteen circle patterns with a diameter of 2 μm were etched on the film surface using a standard photolithography process. The sample was post-baked at 150°C for 5 min to tilt the photoresist edge angle; 60 degrees is the most suitable angle for forming the cones. The ramp was etched by Ar ion milling with an incident angle of 45 degrees, and the ramp-edge surface was modified to form a barrier layer, using an accelerating voltage of 1500 V for 3 min. During the etching process, the sample was rotated. This process led to upside-down conical formations shown in Fig. 1 and Fig. 2. After the ion milling, the photoresist was removed by ultrasonic stirring in acetone and in oxygen plasma of 100 W in a barrel reactor. Every

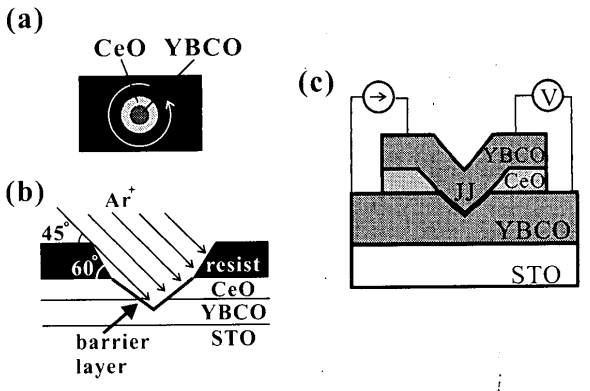

Fig. 1 Schematic images of ion milling to form ramp shape and barrier layer; (a) top view and (b) cross-sectional view. (c) Schematic image of the sample cross section.

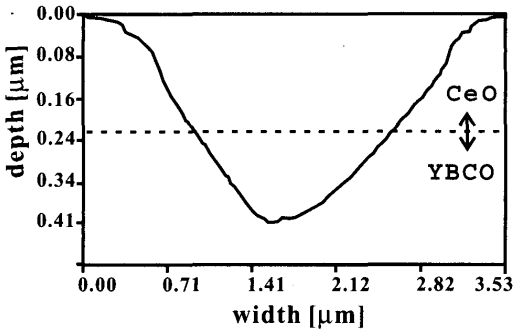

Fig. 2 Cross section of the YBCO/CeO bilayer after ion milling to realize conical formation. The resist mask was reflowed by post-baking at 150°C for 5 min. The slope was between 14 and 18 degrees.

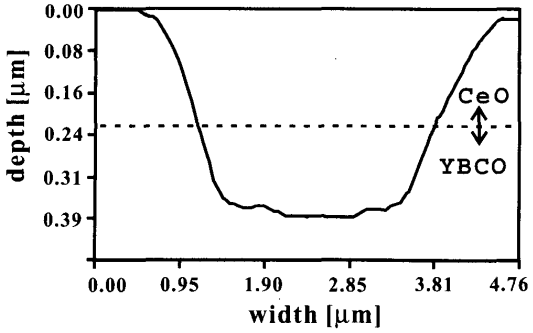

Fig. 3 Cross section of the YBCO/CeO bilayer after ion milling when the resist mask edge angles were less than the incident angle of the ion beam.

junction that did not undergo ion milling to modify the edge surfaces had I_c whose values exceeded the maximum value we can measure (40 mA). This indicates that this process alone is not sufficient to form the barrier layers.

The sample was placed in the deposition chamber again *ex situ*. Annealing for 30 min at 690°C with 200 mTorr oxygen pressure was carried out to recrystallize the amorphous layer on the surface of the etched YBCO. Subsequently, another 250-nm-thick YBCO film for the top electrode was deposited at 690°C with 200 mTorr oxygen pressure.

The junctions themselves were defined by a second photolithography process and Ar ion milling. The resist mask was post-baked at 180°C for 5 min to make the tilt angle of the mask edge less than the incident angle of Ar ion beam, which maintains the distance and ensures the electrical insulation between the wires. The electrical contacts to the bottom electrode were ensured through these processes. A 50-nm-thick gold layer was evaporated to provide electrical contacts. Finally, the sample was annealed at 600°C in 1 atmosphere oxygen for 30 min to reduce the contact resistance between the YBCO film and the gold electrodes.

3. Experimental Results

We have fabricated conical junction formations in order to apply the ramp geometry to the trilayer structures. Figure 2 shows a cross-sectional view of a ramp consisting of a YBCO/CeO bilayer scanned by atomic force microscopy (AFM). The tilt angle of the ramp should be less than 45 degrees to grow c-axis oriented YBCO films on the ramp-edge surfaces [4]. The shape of the ramp has a slope of between 14 and 18 degrees for each junction, and these values were sufficiently low. Four of the junctions in the chip were about 30 nm shallower than the other junctions. This result made a difference of about 2 degrees in the ramp tilt angle.

The sample was rotated during the ion milling, so that all sides of the cone crest were bombarded by Ar ions at all times. Hence, the slope of the ramp was less

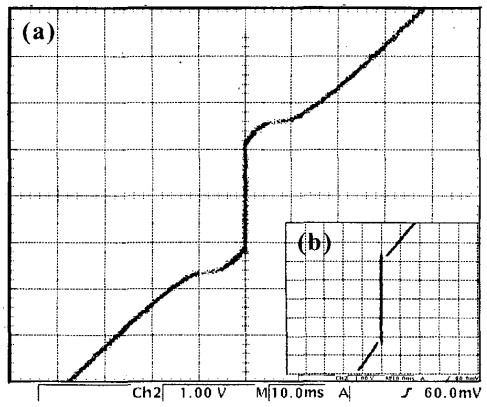

Fig. 4 I-V characteristics of a junction fabricated; (a) at 6.8 K, X = 1 mV/div, Y = 2 mA/div; (b) at 60 K, X = 0.1 mV/div, Y = 0.2 mA/div.

than the ion-beam incident angle of 45 degrees. The junction shapes were determined by the tilt angle and thickness of the resist mask and the incident angle of the ion-beam. When we examined the case in which the tilt angle of the resist mask was less than the incident angle of the ion-beam, the holes were shaped like cups, as shown in Fig. 3. We consider that the cup-like shape is unsuitable for growing the top YBCO layer on the junctions with c-axis orientation.

Figure 4 shows the I-V characteristic of a fabricated junction. The barrier layer was formed by YBCO surface treatment with the ion accelerating voltage of 1500 V for 3 min. We should observe the magnetic response of the junctions to know if the junctions are resistively shunted junction (RSJ) type, but we have not undertaken this yet. Further, the mechanism of formation of the rounding in the low-voltage area shown in Fig. 4 is not yet clear. However, the reason for this can be considered to be that the surfaces of the barrier layers were not clean. Therefore, we will modify the junction surfaces immediately before the top YBCO deposition.

The critical current (I_c) and normal resistance (R_n) were 2.0 mA and 0.5 Ω at 6.8 K, respectively. The temperature dependence of I_c of the junction is shown in Fig. 5. I_c decreased almost linearly as the tempera-

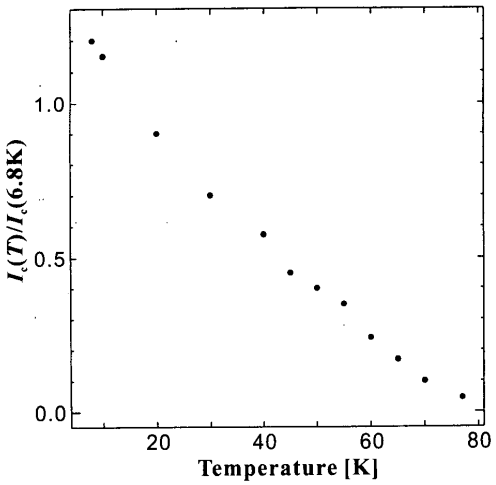

Fig. 5 Temperature dependence of critical current observed for fabricated junction.

ture increased.

We have fabricated sixteen junctions in a chip. Two junctions had I_c values which exceeded our measurement limit, perhaps due to a short circuit between the bottom and top YBCO films in the junctions. Another four junctions showed approximately flux-flow (FF) type I-V characteristics. From the results, we have not yet obtained optimal conditions for forming appropriate barrier layers.

The junction area is a lateral area of a cone. From the result shown in Fig. 2, the height and slope of the cone are about 180 nm and 15 degrees, respectively. Therefore, the junction area is about $1.5 \times 10^{-8}\,\mathrm{cm}^2$. The I_c value mentioned above (2.0 mA) is nearly equal to the I_c values of the flat-type trilayer junctions (1.5 mA) which are 10 μm square [3]. This result implies the effects of ab-plain currents and shows the possibility of decreasing the size of the junction.

4. Conclusions

We have fabricated ramp-type Josephson junctions with trilayer structures. The barrier layers were formed by the interface-modification of the YBCO layer. We have adopted conical shapes for the junctions in order to utilize the ab-plane currents in the trilayer structures. The fabricated junctions showed I-V characteristics which are between RSJ and FF types. We should determine the optimal conditions for forming the barrier layers. However, these results show that the conical shape junctions we fabricated have the potential to be more compact than the flat-type trilayer junctions.

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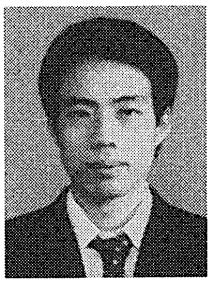

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